What is Claimed is:

1. A ferroelectric memory device, comprising:

a cell array block having a bitline structure including a main bitline and a plurlaity of sub bitlines, the main bitline connected to a column selection controller, and the plurality of sub-bitlines having both terminals connected to the main bitline, respectively, and connected to a plurality of unit cells;

a data bus unit connected to the column selection controller; and

a control circuit unit including a sense amplifier array connected between a data I/O buffer and a sense amplifier data bus connected to the data bus unit,

wherein a plurality of the cell array blocks are arranged like a matrix , the control circuit unit is disposed in a first center line of symmetry wherein the first center line is parallel to the main bitline, and the data bus unit is disposed in a second center line of symmetry wherein the second center line is vertical to the main bitline.

2. The device of claim 1, wherein a plurality of data bus lines included in the data bus unit are connected

one by one to a plurality of the sense amplifier data bus line included in the sense amplifier data bus.

3. The device of claim 1, further comprising a first switch device and a second switch device connected apart in the middle of the data bus unit,

wherein a plurality of the sense amplifier data bus lines in the sense amplifier data bus are connected one by one to a plurality of data bus lines in the data bus unit in a middle region of the first switch device and the second switch device, and electrically connected to one terminal of the data bus unit depending on complementary switching operations of the first and the second switches.

4. The device of claim 1, wherein the data bus unit includes a first data bus unit and a second data bus unit separately disposed from the first data bus unit,

the sense amplifier data bus includes a first sense amplifier data bus connected to the first data bus unit and a second sense amplifier data bus connected the second data but unit,

and each sense amplifier is selectively connected to a data bus line included in the first sense amplifier data bus or a data bus line included in the second sense

amplifier data bus.

5. The device of claim 4, wherein the data bus lines in the first sense amplifier data bus and the second sense amplifier data bus are connected to the sense amplifier via the first switch device and the second switch device, respectively.

6. The device of one of claims 1 to 5, wherein the sense amplifier array includes:

a plurality of sub sense amplifier arrays, each sub sense amplifier comprising a predetermined number of sense amplifiers;

a plurality of local controllers for receiving a column address bit, and outputting a common control signal to a sense amplifier into the predetermined number of sub sense amplifier arrays; and

a global controller for outputting a common control signal into all sense amplifiers in the sense amplifier array.

7. The device of claim 6, wherein the sense amplifier includes:

a data line pull-up controller for pulling up a data

line connected to the sense amplifier data bus line;

an amplification unit for amplifying and storing data inputted into the data line in a read mode or data inputted into an I/O buffer in a write mode; and

an I/O controller for outputting data stored in the amplification unit into the data line in a write mode or into the I/O buffer and the data line in a read mode.

8. The device of claim 7, wherein the amplification unit includes:

a first comparator for comparing the reference signal with a signal of the data line, and outputting a signal of a high level when the signal of the data line has a higher level than the reference signal;

a second comparator for comparing the reference signal with a signal of the data line, and outputting a signal of an opposite level to the first comparator;

a storage unit including a first input terminal connected via an output terminal of the first comparator and a first transmission gate and a second input terminal connected via an output terminal of the second comparator and a second transmission gate, for storing signals inputted into the first and the second input terminals,

wherein the first comparator, the second comparator,

the first transmission gate, the second transmission gate and the storage unit are controlled by the global controller.

9. The device of claim 8, wherein the amplification unit further includes a switch connected between the output terminals of the first comparator and the second comparator, the switch controlled by the global controller.

10. The device of claim 8, wherein the amplification unit further includes a PMOS transistor for pulling up the output terminal of the first comparator when the data line is pulled up.

11. The device of claim 7, wherein the I/O controller includes:

a first path for outputting data inputted from the I/O buffer into the first input terminal of the storage unit, and a complementary value of the inputted data into the second input terminal of the storage unit;

a second path for outputting a value of the second input terminal of the storage unit;

a third path for outputting an output value from the

second path into the I/O buffer; and

a fourth path for outputting an output value from the second path,

wherein the first path, the second path and the third path are controlled by the local controller, and the fourth path is controlled by the global controller.

12. The device of claim 1, wherein the cell array block includes:

a main bitline pull-up controller for pulling up the main bitline in response to a first control signal; and

a cell array connected between the main bitline pull-up controller and the column selection controller.

13. The device of claim 12, wherein the cell array includes:

a main bitline load controller configured to be connected between a positive power and the main bitline, and to control flow of current in response to a second control signal; and

a plurality of sub cell blocks configured to be arranged between the main bitline pull-up controller and the column selection controller, and to be connected to the main bitline in both terminals, respectively.

14. The device of claim 12, wherein the main bitline pull-up controller is a PMOS transistor having a gate to receive the first control signal, a source connected to a positive power and a drain connected to the main bitline.

15. The device of claim 13, wherein the main bitline load controller is connected one by one to the main bitline.

16. The device of claim 13, wherein a plurality of the main bitline load controllers are connected to each main bitline, and evenly placed apart from each other in a predetermined number of sub cell blocks.

17. The device of claim 13, wherein the sub cell block includes:

a first NMOS transistor having a gate connected to a first terminal of the sub bitline, and a drain connected to the main bitline;

a second NMOS transistor having a gate connected to a third control signal, a drain connected to a source of the first NMOS transistor, and a source connected to ground;

a third NMOS transistor having a gate connected to a fourth control signal, a drain connected to a second terminal of the sub bitline, and a source connected to ground;

a fourth NMOS transistor having a gate connected to a fifth control signal, a source connected to the second terminal of the sub bitline, and a drain connected to a sixth control signal; and

a fifth NMOS transistor having a gate connected to a seventh control signal, a drain connected to the main bitline, and a source connected to the second terminal of the sub bitline.

18. The device of one of claims 12 to 17, wherein the connection portion between the column selection controller and the data bus unit includes:

a first layer including the column selection controller having a source connected to the main bitline and a drain connected to a first shared layer;

a second layer including a second shared layer for connecting the first shared layer to a data bus line of the data bus unit; and

a third layer including the data bus unit,

wherein the second layer is disposed below the

first layer and the third layer is disposed below the second layer.

19. The device of claim 1, wherein the ferroelectric memory device further includes:

a first VPP pump circuit; and

a plurality of VPP driving circuits for receiving a VPP from the first VPP pump circuit and outputting the VPP into the cell array block,

wherein the first VPP pump circuit is arranged adjacent to the VPP driving circuit in both end portions of the control circuit unit, and the plurality of the VPP driving circuits are arranged symmetrically with respect to the first VPP pump circuit in each cell array block.

20. The device of claim 19, wherein the VPP driving circuit includes:

a second VPP pump circuit for outputting a gate VPP signal;

a first NMOS transistor having a gate to receive the gate VPP signal outputted from the second VPP pump circuit, and a source to receive an output signal of an address decoder;

a second NMOS transistor having a gate connected to a

drain of the first NMOS transistor, and a drain to receive the VPP outputted from the first VPP pump circuit; and

a third NMOS transistor configured to have a gate controlled by a pull-down control signal and the output signal of the address decoder, a source connected to ground and a drain connected to a source of the second NMOS transistor, and to output a voltage from the drain as a driving voltage.